Calculation of Inrush Currents in Single- and Multi-Step Capacitor Bank Installations

When a capacitor bank is initially connected to a voltage source a transient charging current will flow attempting to equalize the system voltage and the capacitor voltage. If the two voltages are equal at the time of switching, no inrush current flows. If there is a voltage difference across the switch the magnitude and frequency of this inrush current can be calculated. The magnitude and frequency of this charging current depends upon the total capacitance and inductance of the circuit as well as magnitude of the applied voltage. In calculations the crest value of the applied voltage is used and the capacitor voltage is assumed to be zero. While the resistance in the circuit determines the rate at which this transient oscillation decays, it has only a negligible effect upon the initial magnitude and frequency of the transient. In practice the resistance is generally neglected.

The formulas described here are from IEEE Std 1036-2010 *IEEE Guide for Application of Shunt Capacitors*. These formulas provide an accepted analytic approach for estimating the transient currents expected during capacitor switching. The current formulas determine the peak value of the inrush current without damping. In reality, the peak current will be around 90% of the values determined with these formulas. We also include an example that determines the inductance needed to limit the back-to-back transient currents and frequencies based on the circuit breaker capabilities. There are other methods to control these transients in addition to in-line current-limiting reactors --- pre-insertion inductors, pre-insertion resistors, and zero-crossing breaker/control.

Another concern is that, in grounded wye banks, which are common at higher voltages, these high transient currents can raise ground grid potentials and damage other equipment connected to the same ground grid.

The complexity of the system may dictate the need for transient modeling using computer simulation software like EMTP. Given the diversity in system configurations and capacitor bank designs, the engineer may need a more detailed analysis to address the impact of the switching transients and implement a solution to mitigate these transients.

Isolated Banks

The simplest problem is that of a single isolated capacitor bank as shown in Figure 1. Since the short circuit MVA is usually known for any given location on a system, the following simplified expression for the maximum inrush current has been derived based on the available short-circuit MVA. It is assumed that the circuit is closed at crest voltage thereby causing maximum inrush current.

$$I_{\max\ pk} = \frac{1000}{V_{LL}} \times \sqrt{\frac{2}{3}} \times \sqrt{MVA_{SC} x\ MVAR_C}$$ [A] Equation 1

or

$$I_{\max\ pk} = \sqrt{2} \times \sqrt{I_{SC} \times I_C}$$ [A] Equation 2

or

$$I_{\max\ pk} = 1000 \times V_{LL} \times \sqrt{\frac{2}{3}} \times \sqrt{\frac{C}{L_{SC}}}$$ [A] Equation 3

and

$$f_t = \frac{1}{2\pi \times \sqrt{L_{SC} \times C}} = f_S \times \sqrt{\frac{I_{SC}}{I_C}}$$ [Hz] Equation 4

where

$I_{max\ pk}$ = peak inrush current (without damping), in amperes

V_{LL} = maximum line-to-line *rms* voltage in kilovolts

MVA_{SC} = short circuit MVA at the location of the capacitor bank

$MVAR_C$ = capacitor bank Mvar rating

C = capacitor bank capacitance in farads

L_{SC} = system SC inductance in henries

f_t = frequency of the transient in kilohertz

f_s = system frequency, hertz

I_{SC} = available short circuit current at the location of the capacitor, in amperes

I_C = current of the capacitors being switched, in amperes, *rms*

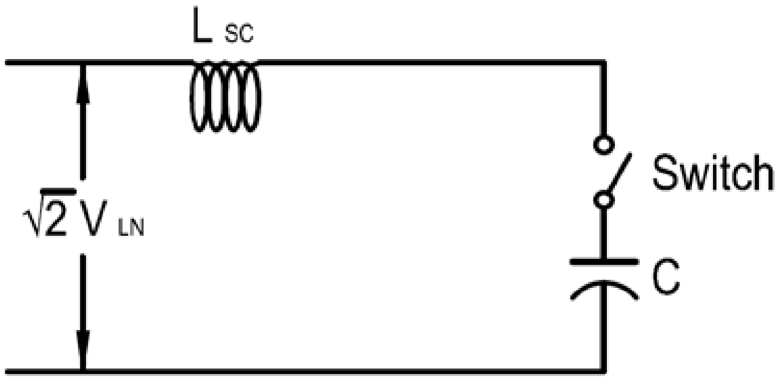

Figure 1. Single isolated capacitor bank

Experience has shown that inrush currents of a single isolated bank normally range from five to 15 times the normal capacitor current. Transient frequencies due to isolated capacitor bank switching generally fall in the 300 Hz to 1000 Hz range.

Parallel Banks

When a capacitor bank is connected in parallel with another bank or banks, an additional inrush current will flow. This is caused by the discharging of the capacitors of the already energized banks into the uncharged bank. While the inrush current from the system is limited by the inductive reactance from the bank to the source, the inrush current from the parallel banks is dependent only upon the inductive reactance between the capacitor steps, and the voltage at the time of switch closing.

It is always assumed that the newly energized step is closed at a system voltage crest and zero voltage on the bank being energized. At this time the capacitor steps already energized have the maximum charge on them which will result in the highest magnitude of inrush current. At voltage crest the current will be at or near zero and if the frequency of the transient is at least 10 times that of the supply voltage nearly all of the inrush current to the newly energized bank will come from the charged parallel banks.

Field experience indicates that the inrush current for multi-step banks is usually between 20 and 250 times the steady-state capacitor current.

The transient current usually decays to some insignificant value in less than one cycle on the system frequency basis (50 or 60 Hz) and often will have decayed to a low value within one-half cycle on the system frequency basis.

In determining the inrush current magnitude and frequency of a two-step capacitor bank refer to Figure 2 and Equations 5 through 10. It is important to remember that the inductance, L_{eq}, is the total inductance, in micro-henry, from the terminal of one capacitor bank to that of the other capacitor bank. This includes the inductance of the lines, the switches, inrush current limiting reactors (if any), and the characteristic inductance of the capacitor bank itself.

A capacitor switch or breaker applied at less than the rated high-frequency transient-making current may be applied at a transient inrush frequency higher than the rated value provided that the rate-of-rise of current (product of $I_{max\ pk} \times f_t$) does not exceed the product of the rated transient inrush frequency of the switch/breaker and the rated high-frequency transient-making current.

$$I_{\max\ pk} = 1000 \times V_{LL} \times \sqrt{\frac{2}{3}} \times \sqrt{\frac{C_{eq}}{L_{eq}}}$$ [A] Equation 5

or

$$I_{\max\ pk} = 1000 \times \sqrt{\frac{2}{3}} \times \sqrt{\frac{\sqrt{3} \times 1000 \times V_{LL} \times (I_1 \times I_2)}{2\pi \times f_S \times L_{eq} \times (I_1 + I_2)}}$$ [A] Equation 6

or

$$I_{\max\ pk} = 13{,}555 \times \sqrt{\frac{V_{LL} \times (I_1 \times I_2)}{f_S \times L_{eq} \times (I_1 + I_2)}}$$ [A] Equation 7

or

$$I_{\max\ pk} = \sqrt{\frac{1000}{3 \times \pi \times f_S}} \times \sqrt{\frac{\frac{MVAR_{C1} \times MVAR_{C2}}{MVAR_{C1} + MVAR_{C2}}}{L_{eq}}}$$ [A] Equation 8

and

$$f_t = \frac{1}{2 \times \pi \times \sqrt{L_{eq} \times C_{eq}}}$$ [Hz] Equation 9

or

$$f_t = \frac{1}{\sqrt{2 \times \pi}} \times \sqrt{\frac{1000 \times f_S \times V_{LL} \times (I_1 + I_2)}{\sqrt{3} \times L_{eq} \times (I_1 \times I_2)}}$$ [Hz] Equation 10

where

$I_{max\ pk}$ = peak inrush current (without damping), in amperes

V_{LL} = maximum line-to-line *rms* voltage in kilovolts

$MVAR_{C1}$ = three-phase Mvar rating of capacitor already energized

$MVAR_{C2}$ = three-phase Mvar rating of capacitor being switched

C_{eq} = equivalent capacitance of the two capacitor banks in series, in farads

L_{eq} = total equivalent inductance per phase between capacitor banks, in henries

f_s = system frequency, in hertz

f_t = frequency of transient inrush current, in hertz

I_1, I_2 = currents of the capacitors being switched, in amperes, *rms*

Figure 2 shows a typical circuit for back-to-back switching. Per IEEE Std C37.012-2014, the inductances within the capacitor banks (L_{C1} and L_{C2}) are of the order of 10 µH for banks above 52 kV and 5µH for banks below 52 kV. IEEE Std C37.66-2005 suggests a value of 0.984 µH per meter of overhead bus or 0.295 µH per meter of cable for L_1, L_2, and L_{bus}. IEEE Std C37.012-2014 lists the typical value of inductance per phase between back-to-back capacitor banks. See Table 1. The inductance of the vacuum or SF_6 switch/circuit breaker is negligible.

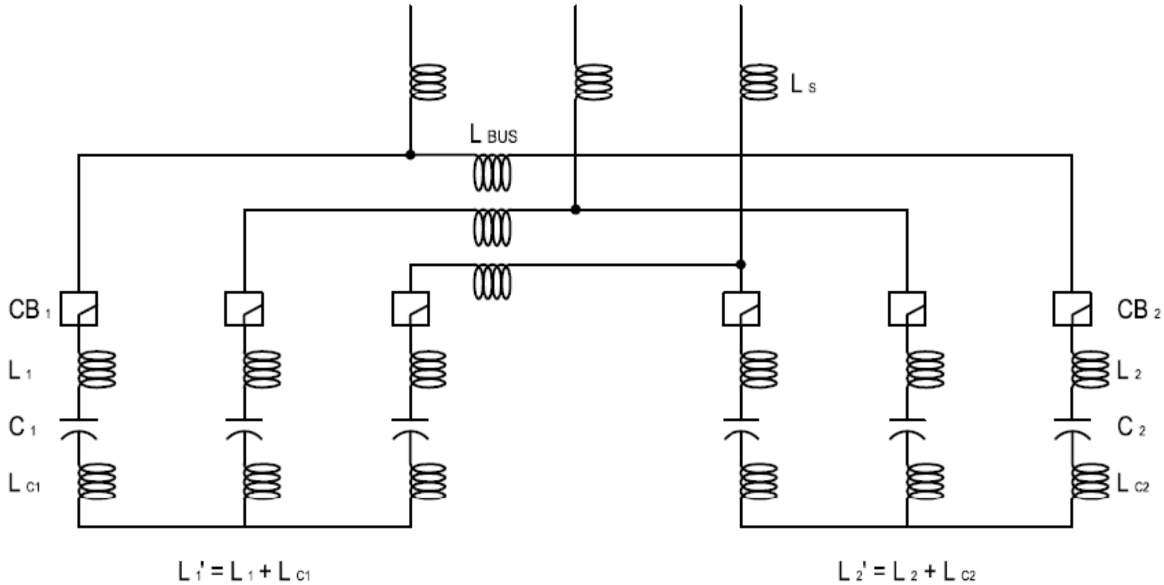

Figure 2. Circuit parameters for back-to-back switching of capacitor banks

Table 1. Typical values of inductance between capacitor banks

Rated maximum voltabe (kV)	Inductance per phase of busbar (µH/m)	Typical inductance between banks (µH)	Total inductance between banks*, L_{eq} (µH)
17.5 and below	0.702	10-20	20-30
36	0.781	15-30	25-40
52	0.840	20-40	30-50
72.5	0.840	25-50	45-70
123	0.856	35-70	55-90
145	0.856	40-80	60-100
170	0.879	60-120	80-140
245	0.935	85-170	105-190
*This value includes the inductance within the capacitor bank itself.			

Example

Calculate the peak energization inrush current and frequency for the capacitor banks at a 115 kV substation (Figure 3). The three capacitor banks are rated 12,000 kvar three-phase each. The separation between the banks is as described in Figure 3. The system short circuit current is 18.8 kA at 123 kV. Circuit breakers CB1 and CB2 have the following characteristics:

Rated Maximum Voltage: 123 kV

Rated Continuous Current: 1200 A, *rms*

Rated Short Circuit Current: 31.5 kA, *rms*

Back-to-Back Capacitor Switching:

Rated Inrush Current: 16 kA, peak

Rated Frequency: 4.3 kHz

Consider the following 3 scenarios:

Scenario 1 – Energization of capacitor bank 1 alone (capacitor banks 2 and 3 de-energized).

Scenario 2 – Energization of capacitor bank 1 with capacitor bank 2 already energized.

Scenario 3 – Energization of capacitor bank 1 with capacitor banks 2 and 3 already energized.

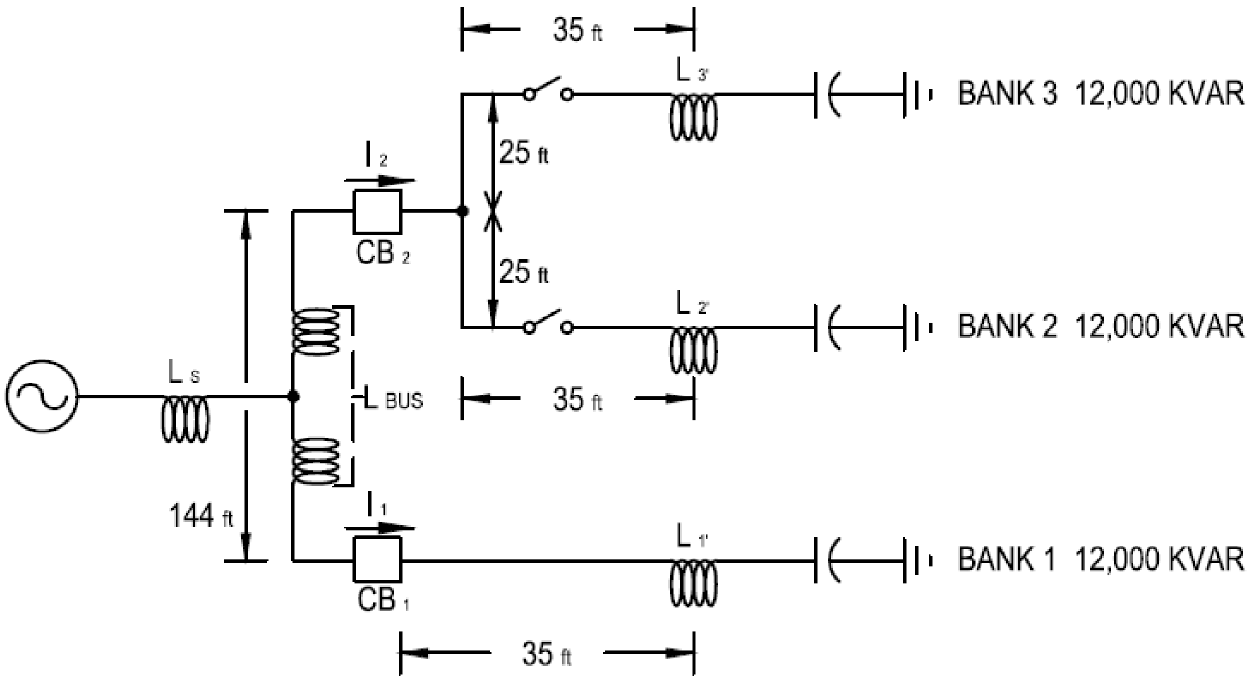

Figure 3. Back-to-back switching of capacitor banks on a 115 kV substation

Capacitor bank nominal current:

$$I_C = \frac{12{,}000}{\sqrt{3} \times 115} = 60 \text{ A}$$

Capacitor Bank Current considering applied voltage (+7%), and capacitance tolerance (+10%):

$$I_C = 60 \times 1.07 \times 1.10 = 71 \text{ A}$$

System short circuit current:

$$I_{SC} = 18{,}800 \text{ A}$$

Table 3. Inductance between capacitor banks for 115 kV example

	Bus/Cable Inductance				Bank Inductance	Total Inductance
	inductance (µH/m)	ft	meters	inductance (µH)	inductance (µH)	inductance including bank (µH)
L_1' =	0.856	35	10.7	9.1	10.0	19.1
L_2' =	0.856	60	18.3	15.7	10.0	25.7
L_3' =	0.856	60	18.3	15.7	10.0	25.7
L_{Bus} =	0.856	144	43.9	37.6	-	37.6

Scenario 1

From Equation 2

$$I_{\max\, pk} = \sqrt{2} \times \sqrt{I_{SC} \times I_C} = 1.4142 \times \sqrt{18{,}800 \times 71} = 1{,}628 \quad \text{A}$$

From Equation 4

$$f_t = f_S \times \sqrt{\frac{I_{SC}}{I_C}} = 60 \times \sqrt{\frac{18{,}800}{71}} = 976 \quad \text{Hz}$$

Scenario 2

$L_{eq} = L_1' + L_{Bus} + L_2'$

$L_1' = 19.1\ \mu\text{H}$

$L_2' = 25.7\ \mu\text{H}$

$L_{Bus} = 37.6\ \mu\text{H}$

$L_{eq} = 19.1 + 25.7 + 37.6 = 82.4\ \mu\text{H}$

From Equation 7

$$I_{\max\, pk} = 13{,}555 \times \sqrt{\frac{V_{LL} \times (I_1 \times I_2)}{f_s \times L_{eq} \times (I_1 + I_2)}} = 13{,}555 \times \sqrt{\frac{V_{LL} \times (71 \times 71)}{f_S \times L_{eq} \times (71 + 71)}}$$

$$= 13{,}555 \times \sqrt{\frac{123 \times 71 \times 71}{60 \times 82.4 \times (71+71)}} = 13{,}555 \times \sqrt{0.88} = 12{,}742 \quad \text{A}$$

From Equation 10

$$f_t = \frac{1}{\sqrt{2 \times \pi}} \times \sqrt{\frac{1000 \times f_S \times V_{LL} \times (I_1 + I_2)}{\sqrt{3} \times L_{eq} \times (I_1 \times I_2)}} = \frac{1}{\sqrt{2 \times \pi}} \times \sqrt{\frac{1000 \times 60 \times 123 \times (71+71)}{\sqrt{3} \times 82.4 \times 71 \times 71}} = 15.23 \quad \text{kHz}$$

The inrush current peak is within the breaker capability but the frequency is higher than what the breaker can handle. Adding an inductance will limit the inrush current and frequency. Adding a reactor of 1.00 mH will limit the inrush current peak to 3,515 A and the frequency to 4.20 kHz, within the capability of the circuit breaker.

Scenario 3

In this case I_1 = 71 A and I_2 = 2 X 71 = 142 and $L_{eq} + L_1' = L_{Bus} + L_2'/2$ = 19.1 + 37.6 + 25.7/2 = 69.5 µH.

From Equation 7

$$I_{\max\, pk} = 13{,}555 \times \sqrt{\frac{V_{LL} \times (I_1 \times I_2)}{f_s \times L_{eq} \times (I_1 + I_2)}} = 13{,}555 \times \sqrt{\frac{123 \times 71 \times 142}{60 \times 69.5 \times (71+142)}} = 16{,}013 \quad \text{A}$$

From Equation 10

$$f_t = \frac{1}{\sqrt{2 \times \pi}} \times \sqrt{\frac{1000 \times f_S \times V_{LL} \times (I_1 + I_2)}{\sqrt{3} \times L_{eq} \times (I_1 \times I_2)}} = \frac{1}{\sqrt{2 \times \pi}} \times \sqrt{\frac{1000 \times 60 \times 123 \times (71+142)}{\sqrt{3} \times 69.5 \times 71 \times 142}} = 14.36 \quad \text{kHz}$$

The inrush current and frequency is higher than what the breaker can handle. Adding an inductance will limit the inrush current and frequency. Adding a reactor of 0.71 mH will limit the inrush current peak to 4,782 A and the frequency to 4.29 kHz, within the capability of the circuit breaker.

Multiple Banks in Parallel

For multiple banks in parallel (Figure 4a) the peak inrush current when energizing the last capacitor bank of N identical banks connected in parallel can be calculated with Equation 11 and the transient frequency with Equation 12.

$$I_{\max\ pk} = 1000\ \times\ V_{LL}\ \times \sqrt{\frac{2}{3}} \times \left(\frac{N-1}{N}\right) \times \sqrt{\frac{C_1}{L_1}}$$ [A] Equation 11

and

$$f_t = \frac{1}{2 \times \pi \times \sqrt{L_1 \times C_1}}$$ [Hz] Equation 12

where

- $I_{max\ pk}$ = peak inrush current (without damping), in amperes
- V_{LL} = maximum line-to-line *rms* voltage in kilovolts
- N = total number of identical banks in parallel
- C_1 = capacitor bank capacitance in farads (one bank)
- L_1 = capacitor bank and bus-work inductance in henries (one bank)
- f_t = frequency of the transient in hertz

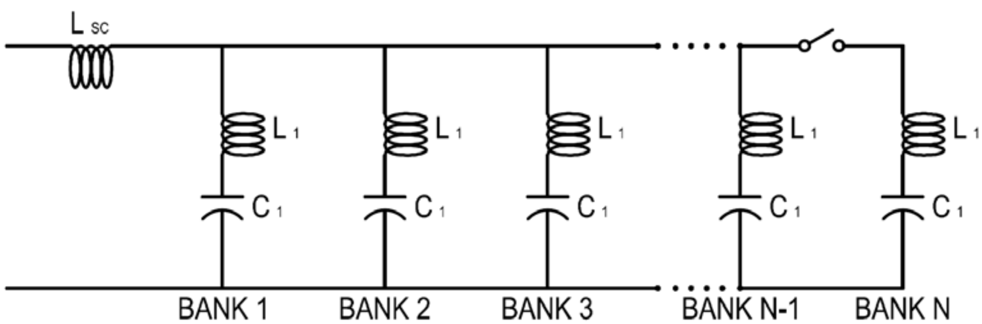

Figure 4a. Multiple similar capacitor banks connected back-to-back

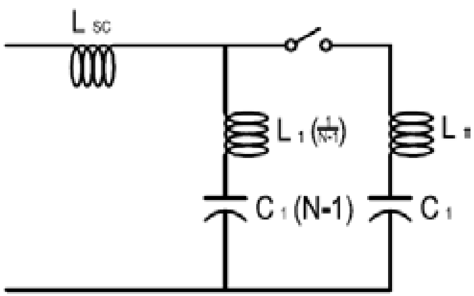

Figure 4b. Simplified back-to-back switching circuit

We can express the peak current for N steps connected in parallel as a multiple of the peak current when N=2.

Table 4. Multiplier for multiparallel equal steps

N	(N-1)/N	Multiplier
2	0.50	Ipk
3	0.67	1.33 x Ipk
4	0.75	1.50 x Ipk
5	0.80	1.60 x Ipk
6	0.83	1.67 x Ipk
...		
∞	1.00	2.00 x Ipk

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