

TLP1013V1

Trans-inductor regulator power inductor



Product features

- Operating frequency range: up to 3 MHz
- Ferrite core material
- 9.6 mm x 6.4 mm footprint surface mount package in a 13.15 mm height
- Inductance range: 105 nH to 170 nH
- Current range: 66 A to 108 A
- 100 Vdc insulation between windings
- Weight: 3.4 g typical
- Moisture sensitivity level (MSL): 1

Applications

- Multi-phase and Vcore regulators
- Voltage regulator modules (VRMs) and high power density VRMs
 - Server and desktop
 - Central processing unit (CPU)
 - Graphics processing unit (GPU)
 - Application specific integrated circuit (ASIC)
- Data networking and storage systems
- Graphics cards and battery power systems
- Point-of-Load modules

Environmental compliance and general specifications

- Storage temperature range (component): -40 °C to +125 °C
- Operating temperature range: -40 °C to +125 °C (ambient plus self-temperature rise)
- Solder reflow temperature: J-STD-020 (latest revision) compliant



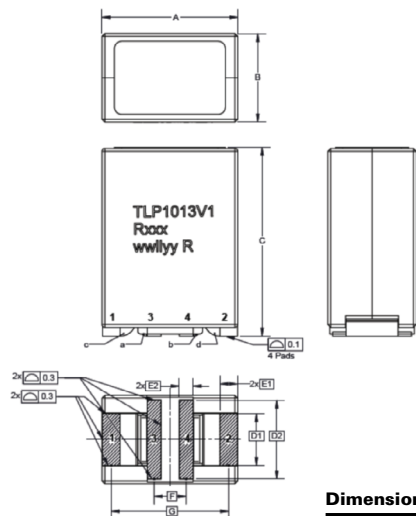
Product specifications

Part number ⁹	Lpri ¹ (nH) ±10%	Lsec ¹ (nH) ±10%	FLL ² (nH) Minimum	I _{sec} ³ (A)	I _{sat} ^{1,4} (A)	I _{sat} ^{2,5} (A)	I _{sat} ^{3,6} (A)	K-factor ⁷	DCR _{pri} (mΩ) @ +20 °C ±10%	DCR _{sec} (mΩ) @ +20 °C ±10%	Kps ⁸ Typical
TLP1013V1-R105-R	105	105	75	72	108	95	87	352	0.53	0.14	0.95
TLP1013V1-R120-R	120	120	86	72	94	83	76	352	0.53	0.14	0.95
TLP1013V1-R150-R	150	150	108	72	75	66	60	352	0.53	0.14	0.96
TLP1013V1-R170-R	170	170	122	72	66	58	53	352	0.53	0.14	0.96

- Open circuit inductance (OCL) test parameters: 100 kHz, 0.1 V_{rms}, 0.0 Adc, +25 °C
- Full load inductance (FLL) test parameters: 100 kHz, 0.1 V_{rms}, I_{sat}1, +25 °C
- I_{sec}: DC current for an approximate temperature rise of 40 °C without core loss. Derating is necessary for AC currents. PCB layout, trace thickness and width, air-flow, and proximity of other heat generating components will affect the temperature rise. It is recommended that the temperature of the part not exceed +125 °C under worst case operating conditions verified in the end application.

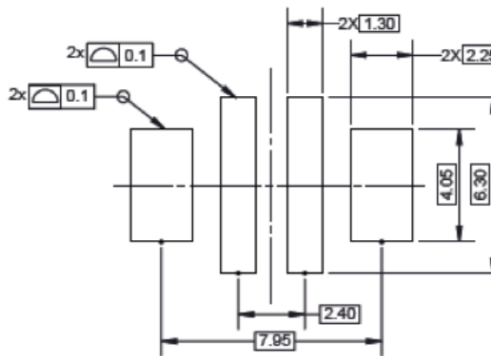
- I_{sat}1 : Peak current for approximately 20% rolloff @ +25 °C
- I_{sat}2 : Peak current for approximately 20% rolloff @ +100 °C
- I_{sat}3 : Peak current for approximately 20% rolloff @ +125 °C
- K-factor: Used to determine Bp-p for core loss (see graph). Bp-p = K * L * ΔI * 10⁻³. Bp-p(Gauss), K: (K-factor from table), L: (Inductance in nH), ΔI (Peak to peak ripple current in Amps).
- Kps: Coupling Coefficient
- Part number definition: TLP1013V1-Rxxx-R
TLP1013 = Product code and size
Vx= Version indicator
Rxxx=Inductance value in uH, R=decimal point
-R suffix = RoHS compliant

Dimensions-mm



Dimension	TLP1013V1-R
A	9.6 maximum
B	6.4 maximum
C	13.15 maximum
D1	3.55
D2	5.4
E1	1.2
E2	0.95
F	2.19
G	8.04

Recommended pad layout



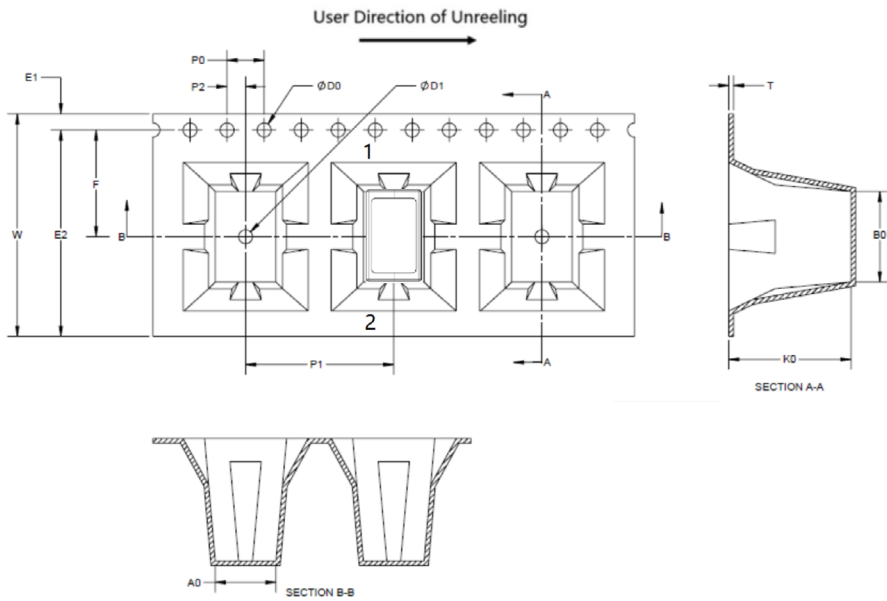
Schematic



Part marking: TLP1013=Product code and size, Vx=Version indicator, Rxxx= inductance value in uH, R=decimal point, xxxx= lot code
Tolerances are ±0.15 millimeters unless stated otherwise
All soldering surfaces to be coplanar within 0.1 millimeters
Pad layout tolerances are ±0.1 millimeters unless stated otherwise
DCR_{pri} is measured from point "a" to point "b"
DCR_{sec} is measured from point "a" to point "b"
Traces or vias underneath the inductor is not recommended
Dimensions of recommended PCB layout are reference only
Add 0.4 mm gap of pad 3 & 4 to avoid short cut issue

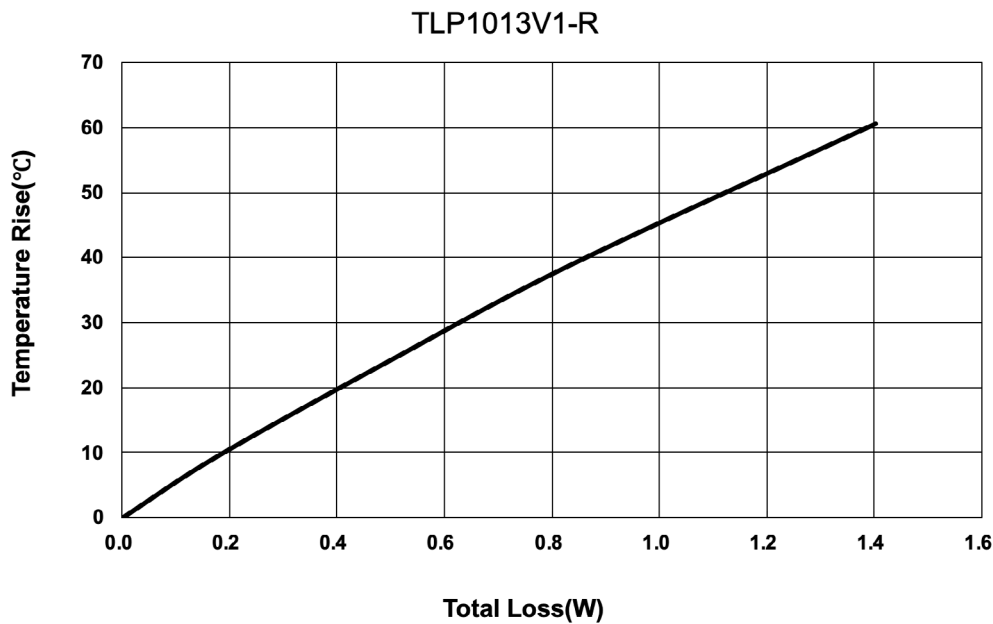
Packaging information- mm

Supplied in tape and reel packaging, 280 parts per 13" diameter reel (EIA-481 compliant)

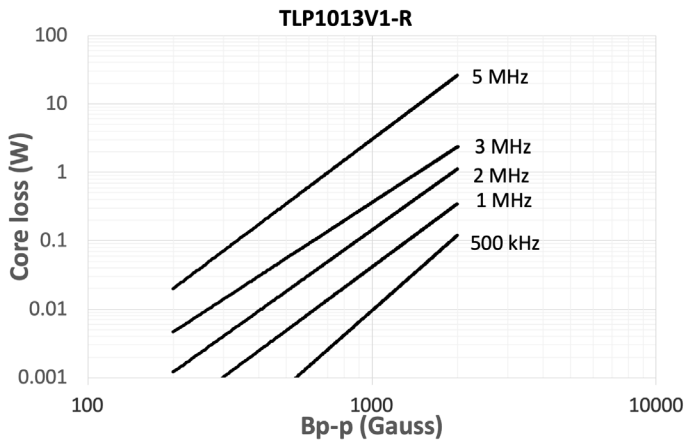


Item	Dimensions
W ± 0.30	24.00
F ± 0.10	11.50
E1 ± 0.10	1.75
E2 minimum	22.25
P0 ± 0.10	4.00
P1 ± 0.10	16.00
P2 ± 0.10	2.00
D0 + 0.10/-0	1.50
D1 minimum	1.50
A0 ± 0.10	6.55
B0 ± 0.10	9.75
K0 ± 0.10	13.35
T ± 0.05	0.50

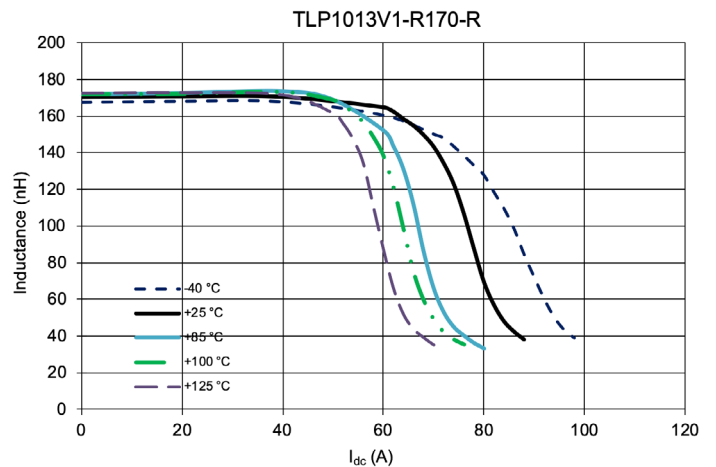
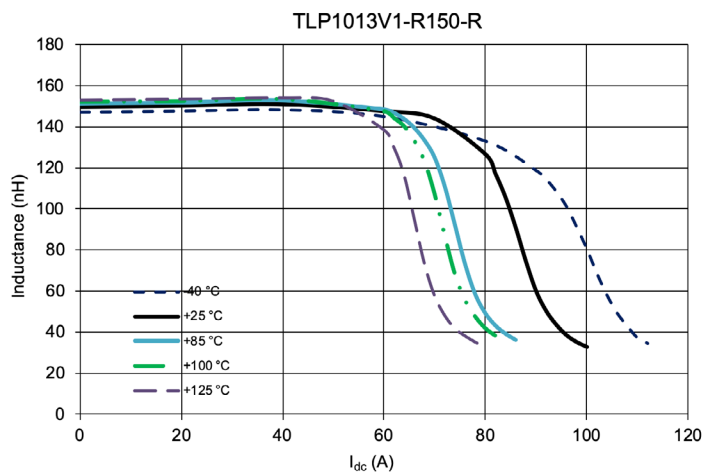
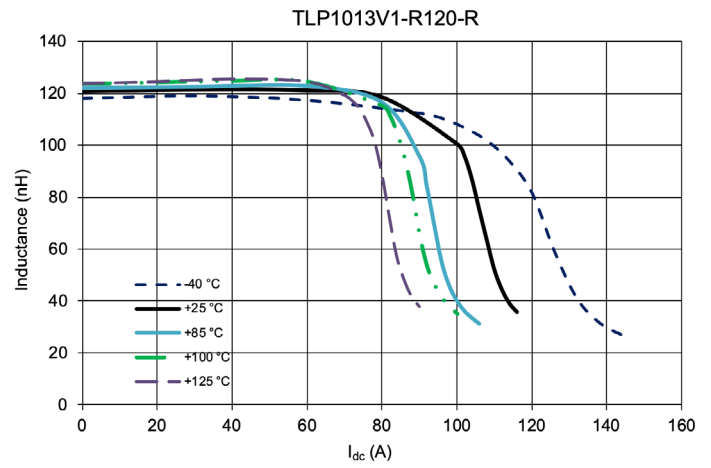
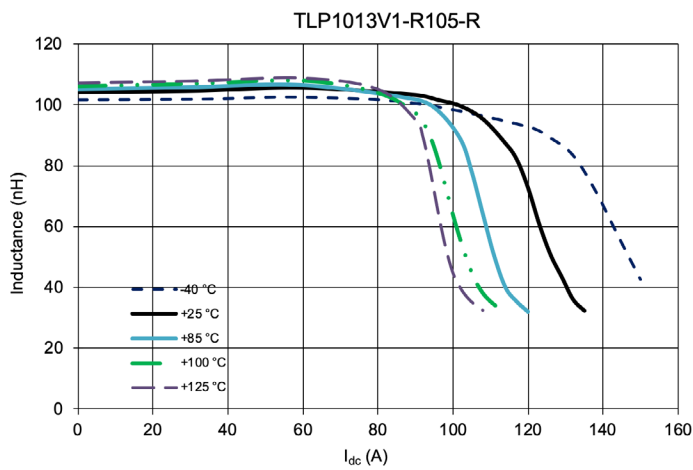
Temperature rise vs. total loss



Core loss vs Bp-p



Inductance characteristics



Solder reflow profile



Table 1 - Standard SnPb solder (T_C)

Package thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2 - Lead (Pb) free solder (T_C)

Package thickness	Volume mm ³ <350	Volume mm ³ 350 - 2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 – 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Reference J-STD-020

Profile feature	Standard SnPb solder	Lead (Pb) free solder
Preheat and soak		
• Temperature min. (T _{smin})	100 °C	150 °C
• Temperature max. (T _{smax})	150 °C	200 °C
• Time (T _{smin} to T _{smax}) (t _s)	60-120 seconds	60-120 seconds
Ramp up rate T _L to T _p	3 °C/ second max.	3 °C/ second max.
Liquidous temperature (T _L)	183 °C	217 °C
Time (t _L) maintained above T _L	60-150 seconds	60-150 seconds
Peak package body temperature (T _p)*	Table 1	Table 2
Time (t _p)* within 5 °C of the specified classification temperature (T _C)	20 seconds*	30 seconds*
Ramp-down rate (T _p to T _L)	6 °C/ second max.	6 °C/ second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

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