TL1211V2 Trans-inductor regulator power inductor



Product features

- Operating frequency range: up to 3 MHz
- · Ferrite core material
- 12 mm x 6.0 mm footprint surface mount package in an 11 mm height
- Inductance range: 70 nH to 200 nH
- Current range: 59 A to 170 A
- 100 Vdc insulation between windings
- Weight: 3.4 g typical
- Moisture sensitivity level (MSL): 1

Applications

- Multi-phase and Vcore regulators
- Voltage regulator modules (VRMs) and high power density VRMs
 - Server and desktop
 - Central processing unit (CPU)
 - Graphics processing unit (GPU)
 - Application specific integrated circuit (ASIC)
- Data networking and storage systems
- · Graphics cards and battery power systems
- · Point-of-Load modules

Environmental compliance and general specifications

- Storage temperature range (component): -40 °C to +125 °C
- Operating temperature range: -40 °C to +125 °C (ambient plus self-temperature rise)
- Solder reflow temperature: J-STD-020 (latest revision) compliant





Technical Data ELX1157 Effective March 2022

Product specifications

Part number ⁹	Lpri ¹ (nH) ±10% (3-4)	Lsec ¹ (nH) ±10% (1-2)	FLL² (nH) Minimum	I _{rms} _sec ³ (A)	l _{sat} 1⁴ (Å)	I _{sat} 2⁵ (Å)	I _{sat} 3 ⁶ (A)	K-factor ⁷	DCR_pri (mΩ) @ +20 °C ±10%	DCR_sec (mΩ) @ +20 °C ±10%	Kps ^₅ Typical
TL1211V2-R070-R	70	70	50	75	170	145	135	328	0.37	0.125	0.93
TL1211V2-R080-R	80	80	57	75	149	127	119	328	0.37	0.125	0.93
TL1211V2-R100-R	100	100	72	75	119	102	95	328	0.37	0.125	0.95
TL1211V2-R110-R	110	110	79	75	108	92	86	328	0.37	0.125	0.95
TL1211V2-R120-R	120	120	86	75	99	84	79	328	0.37	0.125	0.95
TL1211V2-R150-R	150	150	108	75	79	67	63	328	0.37	0.125	0.96
TL1211V2-R170-R	170	170	122	75	70	60	56	328	0.37	0.125	0.96
TL1211V2-R200-R	200	200	144	75	59	50	47	328	0.37	0.125	0.96

1. Open circuit inductance (OCL) test parameters: 100 kHz, 0.1 $\rm V_{rms},$ 0.0 Adc, +25 $^{\circ}\rm C$

2. Full load inductance (FLL) test parameters: 100 kHz, 0.1 V $_{\rm rms}$, $I_{\rm sat}$ 1, +25 °C

3. Imme: DC current for an approximate temperature rise of 40 °C without core loss. Derating is necessary for AC currents.

PCB layout, trace thickness and width, air-flow, and proximity of other heat generating components will affect the temperature rise. It is recommended that the temperature of the part not exceed +125 °C under worst case operating conditions verified in the end application.

4. Isat1 : Peak current for approximately 20% rolloff @ +25 °C

5. I_{sat}2 : Peak current for approximately 20% rolloff @ +100 °C

6. Isat3 : Peak current for approximately 20% rolloff @ +125 °C

7. K-factor: Used to determine Bp-p for core loss (see graph). Bp-p = K * L * ΔI * 10³. Bp-p:(Gauss), K: (K-factor from table), L: (Inductance in nH), ∆I (Peak to peak ripple current in Amps).

8. Kps: Coupling Coefficient

9. Part number definition: TL1211V2-Rxxx-R

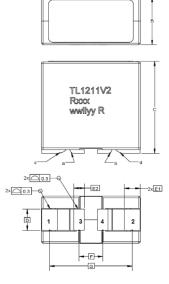
TL1211 = Product code and size

Vx= Version indicator

Rxxx=Inductance value in µH, R=decimal point

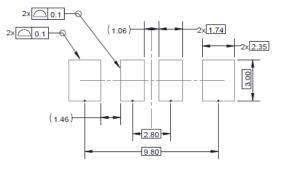
-R suffix = RoHS compliant

Dimensions-mm

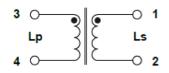


Dimension	TL1211V2-R		
A	12.0 maximum		
В	6.0 maximum		
С	11.0 maximum		
D	2.55		
E1	1.8		
E2	1.24		
F	2.79		
G	9.8		

Recommended pad layout



Schematic



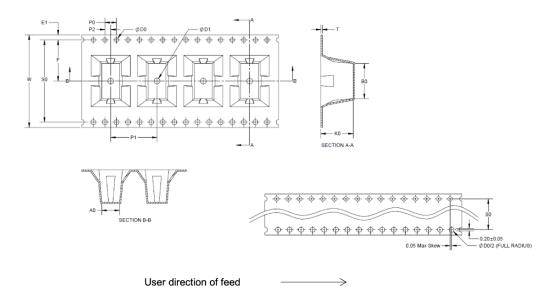
Part marking: TL1211=Product code and size, Vx=Version indicator, Rxxx= inductance value in uH, R=decimal point, xxxx= lot code Tolerances are ±0.15 millimeters unless stated otherwise All soldering surfaces to be coplanar within 0.1 millimeters Pad layout tolerances are ±0.1 millimeters unless stated otherwise DCR_pri is measured from point "a" to point "b" DCR_sec is measured from point "a" to point "b" Traces or vias underneath the inductor is not recommended Dimensions of recommended PCB layout are reference only

2 www.eaton.com/electronics

Add 0.4 mm gap of pad 3 & 4 to avoid short cut issue

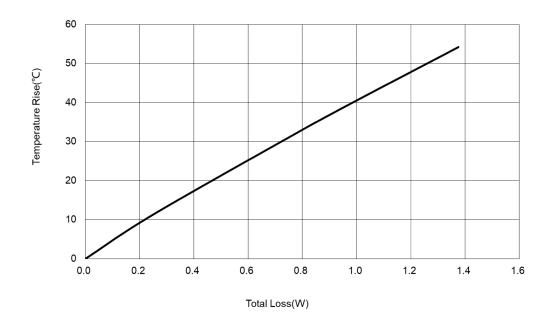
Packaging information- mm

Supplied in tape and reel packaging, 350 parts per 13" diameter reel (EIA-481 compliant)

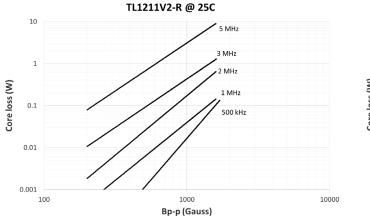


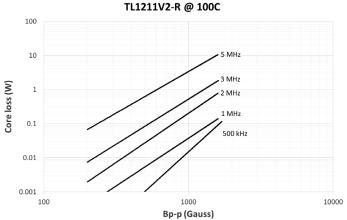
ltem	Dimensions
W ± 0.30	32.00
F ± 0.10	14.20
E1 ± 0.10	1.75
E2 minimum	28.40
P0 ± 0.10	4.00
P1 ± 0.10	16.00
P2 ± 0.10	2.00
D0 + 0.10/-0	1.50
D1 minimum	2.00
A0 ± 0.10	6.15
B0 ± 0.10	12.15
K0 ± 0.10	11.20
T ± 0.05	0.50

Temperature rise vs. total loss

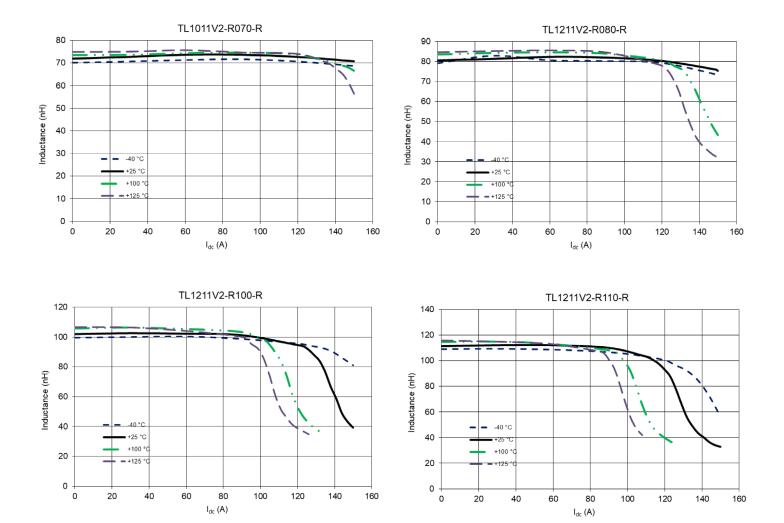


Core loss vs Bp-p



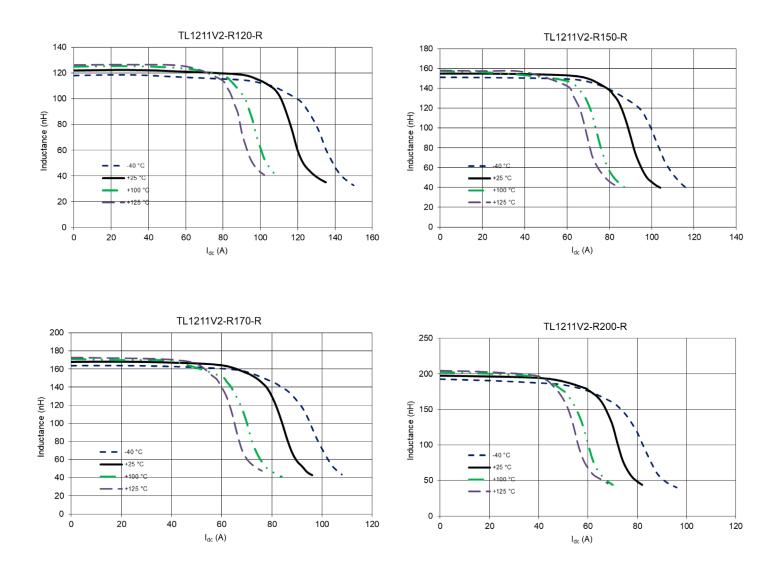


Inductance characteristics



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Inductance characteristics



Solder reflow profile

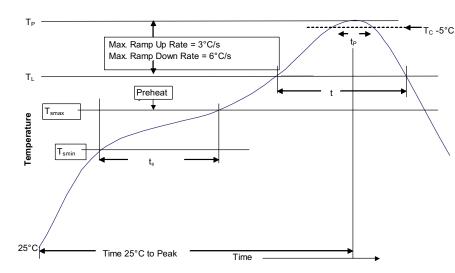


Table 1 - Standard SnPb solder (T_c)

Package thickness	Volume mm3 <350	Volume mm3 ≥350
<2.5 mm)	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2 - Lead (Pb) free solder (T_c)

\	Package thickness	Volume mm ³ <350	Volume mm ³ 350 - 2000	Volume mm ³ >2000
	<1.6 mm	260 °C	260 °C	260 °C
	1.6 – 2.5 mm	260 °C	250 °C	245 °C
	>2.5 mm	250 °C	245 °C	245 °C

Reference J-STD-020

Powerina Business Worldwide

Profile feature	Standard SnPb solder	Lead (Pb) free solder 150 °C	
Preheat and soak • Temperature min. (T _{smin})	100 °C		
• Temperature max. (T _{smax})	150 °C	200 °C	
• Time (T _{smin} to T _{smax}) (t _s)	60-120 seconds	60-120 seconds	
Ramp up rate T _L to T _p	3 °C/ second max.	3 °C/ second max.	
Liquidous temperature (TL) Time (tL) maintained above TL	183 °C 60-150 seconds	217 °C 60-150 seconds	
Peak package body temperature (Tp)*	Table 1	Table 2	
Time $(t_p)^*$ within 5 °C of the specified classification temperature (T_c)	20 seconds*	30 seconds*	
Ramp-down rate (Tp to TL)	6 °C/ second max.	6 °C/ second max.	
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.	

 * Tolerance for peak profile temperature (T_D) is defined as a supplier minimum and a user maximum.

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Eaton Electronics Division 1000 Eaton Boulevard Cleveland, OH 44122 United States Eaton.com/electronics

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