TL1211V1 Trans-inductor regulator power inductor



Product features

- Operating frequency range: up to 3 MHz
- · Ferrite core material
- 12 mm x 6.0 mm footprint surface mount package in an 11.5 mm height
- Inductance range: 70 nH to 200 nH
- Current range: 62 A to 180 A
- 100 Vdc insulation between windings
- Weight: 3.4 g typical
- Moisture sensitivity level (MSL): 1

Applications

- Multi-phase and Vcore regulators
- Voltage regulator modules (VRMs) and high power density VRMs
 - Server and desktop
 - Central processing unit (CPU)
 - Graphics processing unit (GPU)
 - Application specific integrated circuit (ASIC)
- Data networking and storage systems
- · Graphics cards and battery power systems
- · Point-of-Load modules

Environmental compliance and general specifications

- Storage temperature range (component): -40 °C to +125 °C
- Operating temperature range: -40 °C to +125 °C (ambient plus self-temperature rise)
- Solder reflow temperature: J-STD-020 (latest revision) compliant





Technical Data ELX1156 Effective March 2022

Product specifications

Lpri ¹ (nH) ±10% (3-4)_	Lsec ¹ (nH) ±10% (1-2)	FLL² (nH) Minimum	I _{.ms} _S³ (A)	l _{sa,} 1⁴ (Å)	I _{sat} 2⁵ (Å)	I3 ⁶ (Å)	K-factor ⁷	DCR_pri (mΩ) @ +20 °C ±10%	DCR_sec (mΩ) @ +20 °C ±10%	Kps ⁸ Typical
70	70	50	75	180	156	143	313	0.6	0.125	0.93
80	80	57	75	157	137	125	313	0.6	0.125	0.93
100	100	72	75	126	109	100	313	0.6	0.125	0.95
110	110	79	75	114	99	91	313	0.6	0.125	0.95
120	120	86	75	105	91	84	313	0.6	0.125	0.95
150	150	108	75	84	73	67	313	0.6	0.125	0.96
170	170	122	75	74	64	59	313	0.6	0.125	0.96
200	200	144	75	62	53	48	313	0.6	0.125	0.96
	(i)+H) ±10% (3-4)_ 70 80 100 110 110 120 150 170	(jH) ±10% (jH) ±10% 70 70 80 80 100 100 110 110 120 120 150 150 170 170	Image Image Image Image 70 70 50 80 80 57 100 100 72 110 110 79 120 120 86 150 150 108 170 170 122	Image Image <th< td=""><td>Image Image <th< td=""><td>Image Image <th< td=""><td>ÎNH) ±10%INH) ±10%INH) ±10%INH ±10%INH ±10%INH ±10%INH ±10%INH ±10%7070507518015614380805775157137125100100727512610910011011079751149991120120867510591841501501087584736717017012275746459</td><td>Î(1)10%I(1)I(1</td><td>Lpri (mA) ±10%Lsec' minimumLL2 minimumLm S3Lm 14Lm 25Lm 36Lm 36Lm 36Lm 37Lm 37<!--</td--><td>Lpri (m4) ±10%Lsec' (m1) ±10%FLL2 (m1) ±10%FLL2 (m1)FLL2 (m1)FLL2 (m1)DCR sec (m2) ±10%DCR sec (m2) ±10%<</td></td></th<></td></th<></td></th<>	Image Image <th< td=""><td>Image Image <th< td=""><td>ÎNH) ±10%INH) ±10%INH) ±10%INH ±10%INH ±10%INH ±10%INH ±10%INH ±10%7070507518015614380805775157137125100100727512610910011011079751149991120120867510591841501501087584736717017012275746459</td><td>Î(1)10%I(1)I(1</td><td>Lpri (mA) ±10%Lsec' minimumLL2 minimumLm S3Lm 14Lm 25Lm 36Lm 36Lm 36Lm 37Lm 37<!--</td--><td>Lpri (m4) ±10%Lsec' (m1) ±10%FLL2 (m1) ±10%FLL2 (m1)FLL2 (m1)FLL2 (m1)DCR sec (m2) ±10%DCR sec (m2) ±10%<</td></td></th<></td></th<>	Image Image <th< td=""><td>ÎNH) ±10%INH) ±10%INH) ±10%INH ±10%INH ±10%INH ±10%INH ±10%INH ±10%7070507518015614380805775157137125100100727512610910011011079751149991120120867510591841501501087584736717017012275746459</td><td>Î(1)10%I(1)I(1</td><td>Lpri (mA) ±10%Lsec' minimumLL2 minimumLm S3Lm 14Lm 25Lm 36Lm 36Lm 36Lm 37Lm 37<!--</td--><td>Lpri (m4) ±10%Lsec' (m1) ±10%FLL2 (m1) ±10%FLL2 (m1)FLL2 (m1)FLL2 (m1)DCR sec (m2) ±10%DCR sec (m2) ±10%<</td></td></th<>	ÎNH) ±10%INH) ±10%INH) ±10%INH ±10%INH ±10%INH ±10%INH ±10%INH ±10%7070507518015614380805775157137125100100727512610910011011079751149991120120867510591841501501087584736717017012275746459	Î(1)10%I(1)I(1	Lpri (mA) ±10%Lsec' minimumLL2 minimumLm S3Lm 14Lm 25Lm 36Lm 36Lm 36Lm 37Lm 37 </td <td>Lpri (m4) ±10%Lsec' (m1) ±10%FLL2 (m1) ±10%FLL2 (m1)FLL2 (m1)FLL2 (m1)DCR sec (m2) ±10%DCR sec (m2) ±10%<</td>	Lpri (m4) ±10%Lsec' (m1) ±10%FLL2 (m1) ±10%FLL2 (m1)FLL2 (m1)FLL2 (m1)DCR sec (m2) ±10%DCR sec (m2) ±10%<

1. Open circuit inductance (OCL) test parameters: 100 kHz, 0.1 $\rm V_{rms},$ 0.0 Adc, +25 $^{\circ}\rm C$

2. Full load inductance (FLL) test parameters: 100 kHz, 0.1 V $_{\rm rms'}$ I $_{\rm sat}$ 1, +25 °C

3. Imm. DC current for an approximate temperature rise of 40 °C without core loss. Derating is necessary for AC currents.

PCB layout, trace thickness and width, air-flow, and proximity of other heat generating components will affect the temperature rise. It is recommended that the temperature of the part not exceed +125 °C under worst case operating conditions verified in the end application.

4. $I_{sat}1$: Peak current for approximately 20% rolloff @ +25 $^{\circ}\text{C}$

5. I_{sat}2 : Peak current for approximately 20% rolloff @ +100 °C

6. Isat3 : Peak current for approximately 20% rolloff @ +125 °C

7. K-factor: Used to determine Bp-p for core loss (see graph). Bp-p = K * L * ΔI * 10⁻³. Bp-p:(Gauss), K: (K-factor from table), L: (Inductance in nH), ΔI (Peak to peak ripple current in Amps).

8. Kps: Coupling Coefficient

9. Part number definition: TL1211V1-Rxxx-R

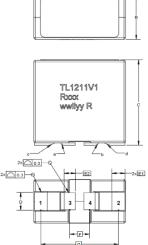
TL1211 = Product code and size

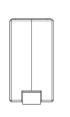
Vx= Version indicator

Rxxx=Inductance value in µH, R=decimal point

-R suffix = RoHS compliant

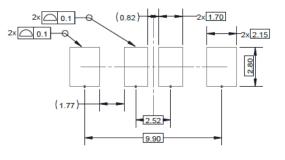
Dimensions-mm



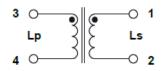


Dimension	TL1211V1-R		
A	12.0 maximum		
В	6.0 maximum		
С	11.05 maximum		
D	2.30		
E1	1.65		
E2	1.42		
F	2.52		
G	9.9		

Recommended pad layout



Schematic



Part marking: TL1211=Product code and size, Vx=Version indicator, Rxxx= inductance value in uH, R=decimal point, xxxx= lot code Tolerances are ±0.15 millimeters unless stated otherwise All soldering surfaces to be coplanar within 0.1 millimeters Pad layout tolerances are ±0.1 millimeters unless stated otherwise DCR_pri is measured from point "a" to point "b" DCR_sec is measured from point "a" to point "b" Traces or vias underneath the inductor is not recommended Dimensions of recommended PCB layout are reference only

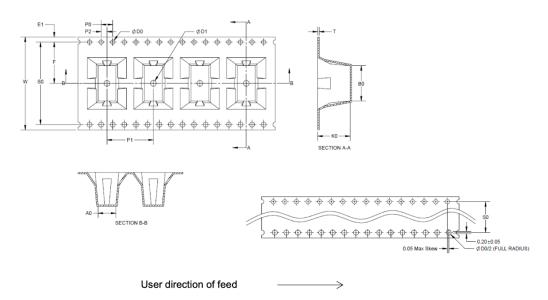
2 www.eaton.com/electronics

Add 0.4 mm gap of pad 3 & 4 to avoid short cut issue

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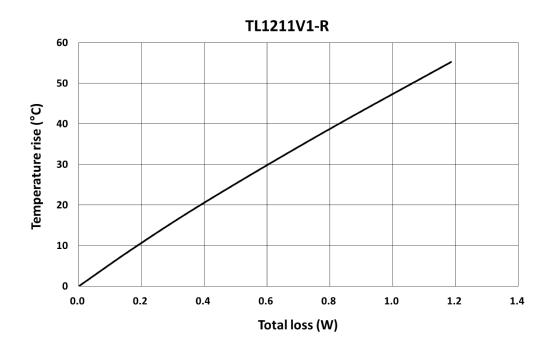
Packaging information- mm

Supplied in tape and reel packaging, 350 parts per 13" diameter reel (EIA-481 compliant)

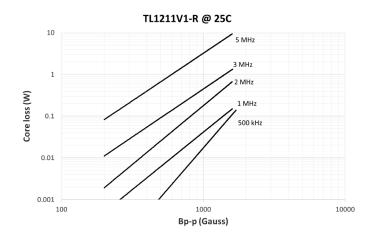


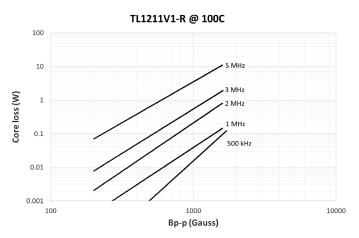
ltem	Dimensions
W ± 0.30	32.00
F ± 0.10	14.20
E1 ± 0.10	1.75
E2 minimum	28.40
P0 ± 0.10	4.00
P1 ± 0.10	16.00
P2 ± 0.10	2.00
D0 + 0.10/-0	1.50
D1 minimum	2.00
A0 ± 0.10	6.15
B0 ± 0.10	12.15
K0 ± 0.10	11.20
T ± 0.05	0.50

Temperature rise vs. total loss

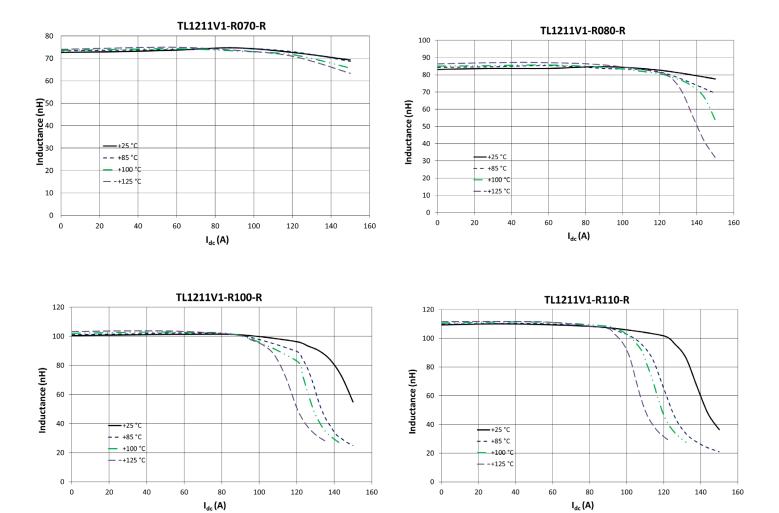


Core loss vs Bp-p



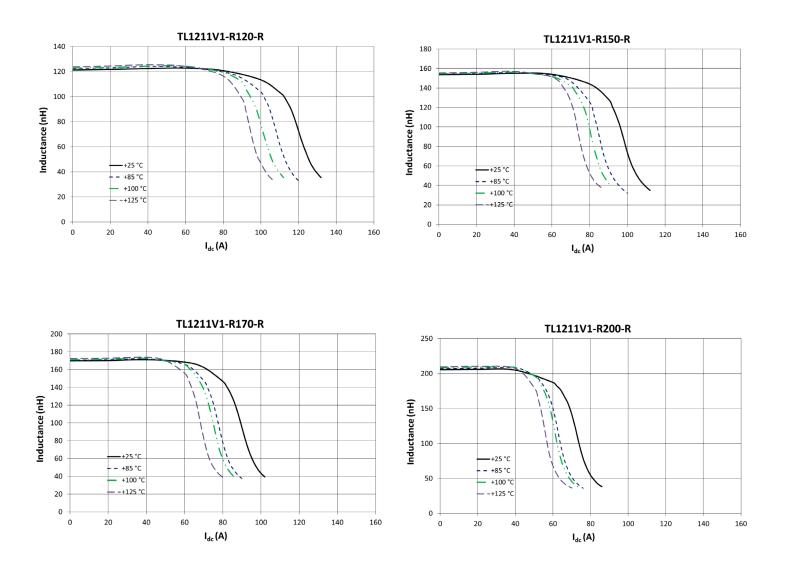


Inductance characteristics



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Inductance characteristics



Solder reflow profile

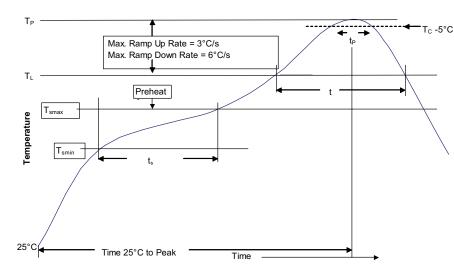


Table 1 - Standard SnPb solder (T_c)

Package thickness	Volume mm3 <350	Volume mm3 ≥350	
<2.5 mm)	235 °C	220 °C	
≥2.5 mm	220 °C	220 °C	

Table 2 - Lead (Pb) free solder (T_c)

\	Package thickness	Volume mm ³ <350	Volume mm ³ 350 - 2000	Volume mm ³ >2000
	<1.6 mm	260 °C	260 °C	260 °C
	1.6 – 2.5 mm	260 °C	250 °C	245 °C
	>2.5 mm	250 °C	245 °C	245 °C

Reference J-STD-020

Powerina Business Worldwide

Standard SnPb solder	Lead (Pb) free solder	
100 °C		
150 °C	200 °C	
60-120 seconds	60-120 seconds	
3 °C/ second max.	3 °C/ second max.	
183 °C 60-150 seconds	217 °C 60-150 seconds	
Table 1	Table 2	
20 seconds*	30 seconds*	
6 °C/ second max.	6 °C/ second max.	
6 minutes max.	8 minutes max.	
	100 °C 150 °C 60-120 seconds 3 °C/ second max. 183 °C 60-150 seconds Table 1 20 seconds* 6 °C/ second max.	

 * Tolerance for peak profile temperature (T_D) is defined as a supplier minimum and a user maximum.

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